

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions.

1. (Currently Amended) ~~Bi~~**A bi-stable latch** circuit having a pair of cross-coupled branches (~~I,H~~), each branch including a complementary driver and a load connected between a drain line and a source line, and **each branch also including** a non-volatile memory cell having a program transistor and a read transistor, **comprising:**

at least one of ~~said~~**the** drivers and loads ~~including said~~**includes a corresponding** read transistor;~~;~~

said driver and load of said branch **are** connected in series at a respective output node;~~;~~

said read transistor and program transistor ~~having~~**have** a common floating gate and separate control gates;~~;~~

said control gate of said program transistor **is** connected to a program voltage;~~;~~

the drain of said program transistor connected to a respective input node;~~;~~ **and**

said control gate of said read transistor in said branch **is** connected to ~~said~~**the** output node of the other branch(~~H~~).

2. (Currently Amended) ~~Latch~~**The bi-stable latch** circuit according to claim 1, wherein at least one of said read transistor or program transistor is a semiconductor device using hot electron injection for changing a threshold voltage thereof.

3. (Currently Amended) ~~Latch~~**The bi-stable latch** circuit according to claim 1 ~~or claim 2~~, wherein said drain and source line are connected across a common supply voltage in static mode but at least one of said drain and source line is disconnected from said common supply voltage in a program mode.

4. (Currently Amended) ~~Latch~~**The bi-stable latch** circuit according to claim 1, wherein the inputs are held at logic low level in said static mode but the voltage at one of said inputs is raised to a voltage high enough to generate hot electrons or hot holes at the drain of a respective program transistor in a program mode.

5. (Currently Amended) ~~Latch~~The latch circuit according to claim 4, wherein said program voltage is connected to said supply voltage in said static mode but said program voltage is raised to a voltage high enough to attract electrons or holes into said floating gate in said program mode.

6. (Cancelled)

7. (Currently Amended) ~~Method~~A method for programming a ~~Bi-stable Latch circuit according to claim 1, wherein said inputs are held at logic low level in said~~bi-stable latch circuit, the bi-stable latch circuit having a pair of cross-coupled branches, each branch including a complementary driver and a load connected between a drain line and a source line, and each branch also including a non-volatile memory cell having a program transistor and a read transistor, comprisingaccording to claim 1 comprising:
_____ holding the input voltages at logic low level in a static mode ~~but the voltage at one of said inputs is raised; and~~
_____ raising the input voltages to a voltage high enough to generate hot electrons or hot holes at the drain of a respective ~~program~~ transistor in a program mode.

8. (Currently Amended) ~~Method~~The method according to claim 7, ~~wherein said~~7 further comprising:

_____ connecting the program voltage ~~is connected to said~~the supply voltage in ~~said~~ static mode ~~but said;~~ and

_____ raising program voltage ~~is raised~~ to a voltage high enough to attract electrons or holes into ~~said~~the floating gate in ~~said~~ program mode.

9. (New) The bi-stable latch circuit according to claim 2, wherein said drain and source line are connected across a common supply voltage in static mode but at least one of said drain and source line is disconnected from said common supply voltage in a program mode.